CLAIMS

What is claimed is:

1. A memory cell with at least two detectable states among which is an unprogrammed state, comprising:

a first branch in series between first and second terminals of application of a read voltage, the first branch including:

a pre-read stage comprising, in parallel, two switchable resistors having different values with a predetermined first difference; and

a programming stage that includes a polysilicon first programming resistor having a terminal accessible by a first programming circuit capable of causing an irreversible decrease in a resistance value of the first programming resistor.

2. The memory cell of claim 1, wherein said decrease in the programming resistance value is predetermined and chosen to be greater than said first difference between the resistances of the pre-read stage.

3. The memory cell of claim 1, wherein the first programming circuit includes switches capable of applying a programming voltage greater than the read voltage across the first programming resistor.

4. The memory cell of claim 1, comprising at least one switch for isolating the pre-read stage with respect to the programming stage.

5. The memory cell of claim 1, wherein a reading of the cell state is performed in two successive steps during which said switchable resistors of the pre-read stage are alternately selected.

6. The memory cell of claim 5, wherein said terminal of the first programming resistor forms a read terminal of the cell capable of being connected to a first terminal of a read amplifier having a second terminal receiving at least one reference voltage chosen to be an intermediary level between the voltage level taken by the read terminal in the two read phases, while the first programming resistor is in an unprogrammed state.

7. The memory cell of claim 1, wherein the first branch includes a first transistor, the memory cell further comprising a second branch that includes a pre-read stage comprising, in parallel, two switchable resistors having different values with a predetermined first difference; a programming stage that includes a polysilicon second programming resistor having a terminal accessible by a second programming circuit capable of causing the irreversible decrease in a resistance value of the second programmable resistor; and a second transistor assembled as a flip-flop with the first transistor, the first programming resistor being connected to the second terminal by the second transistor and the second programming resistor being connected to the second terminal by the first transistor.

8. The memory cell of claim 7, wherein the switchable resistors of the second branch are controllable at the same time as the switchable resistors of the first branch, so that the respective values of the resistors selected in each of the branches are inverted.

9. The memory cell of claim 7, wherein the irreversible decrease to be applied to the programming resistors is chosen to be greater than the sum of the difference between the pre-read resistances and of a third nominal value difference between the programming resistors in an unprogrammed state.

10. A method for reading a memory cell with at least two detectable states among which is an unprogrammed state, the memory cell including a first branch in series between first and second terminals of application of a read voltage, the first branch including: a pre-read stage comprising, in parallel, two switchable resistors having different values with a predetermined first difference; and a programming stage that includes a polysilicon first programming resistor having a terminal accessible by a first programming circuit capable of causing an irreversible decrease in a resistance value of the first programming resistor, the method comprising performing two successive read steps during which said switchable resistors of the pre-read stage are respectively selected.

11. A method for reading a memory cell with first and second memory states, the memory cell including a programmable resistance, the method comprising:

driving the programmable resistance with a first current and measuring a first electrical quantity at the programmable resistance;

driving the programmable resistance with a second current and measuring a second electrical quantity at the programmable resistance; and

detecting the first and second memory states by comparing the first electrical quantity with the second electrical quantity.

12. The method of claim 11 wherein the detecting step includes:

detecting the first memory state by detecting that the first electrical quantity logically equals the second electrical quantity; and

detecting the second memory state by detecting that the first electrical quantity does not logically equal the second electrical quantity.

13. The method of claim 12 wherein detecting the first memory state includes detecting that the first and second electrical quantities are logical high values,

the method further comprising detecting a third memory state by detecting that the first and second electrical quantities are logical low values.

14. The method of claim 11 wherein the detecting step includes:

detecting the first memory state by detecting that the first electrical quantity is greater than the second electrical quantity; and

detecting the second memory state by detecting that the first electrical quantity is less than the second electrical quantity.

15. A memory device, comprising:

a memory cell that includes a programmable resistance;

means for driving the programmable resistance with a first current and measuring a first electrical quantity at the programmable resistance;

means for driving the programmable resistance with a second current and measuring a second electrical quantity at the programmable resistance; and

means for detecting the first and second memory states by comparing the first electrical quantity with the second electrical quantity.

16. The memory device of claim 15 wherein the detecting means includes:

means for detecting the first memory state by detecting that the first electrical quantity logically equals the second electrical quantity; and

means for detecting the second memory state by detecting that the first electrical quantity does not logically equal the second electrical quantity.

17. The memory device of claim 16 wherein the means for detecting the first memory state includes means for detecting that the first and second electrical quantities are logical high values, the memory device further comprising means for

detecting a third memory state by detecting that the first and second electrical quantities are logical low values.

18. The memory device of claim 15 wherein the detecting means includes:

means for detecting the first memory state by detecting that the first electrical quantity is greater than the second electrical quantity; and

means for detecting the second memory state by detecting that the first electrical quantity is less than the second electrical quantity.

19. A memory device, comprising:

memory cell with first and second memory states among which is an unprogrammed state, the memory cell including:

first and second switchable resistance legs coupled in parallel with each other and having different resistance values with a predetermined first difference; and

a first programming resistor connected to the resistance legs and having an unprogrammed, first resistance value and a programmed, second resistance value; and

a first programming circuit connected to the first programming resistor and structured to cause the first programming resistor to change from the first resistance value to the second resistance value.

20. The memory device of claim 19, wherein the difference between the first and second resistance values is predetermined and chosen to be greater than the first difference between the resistance values of the resistance legs.

21. The memory device of claim 19, further comprising an output stage coupled to the first programming resistor and structured to output a state of the memory

cell that depends on a comparison of first and second output levels of the memory cell, the first output level occurring when the first switchable resistance leg is connected in series with the first programming resistor and the second output level occurring when the second switchable resistance leg is connected in series with the first programming resistor.

22. The memory device of claim 19, further comprising a read amplifier having a first input terminal connected to the first programming resistor and a second input terminal connected to a reference voltage chosen to be an intermediary level between a logic high voltage level and a logic low voltage level.

23. The memory device of claim 19, wherein first and second resistance legs and the first programming resistance are part of a first branch that also includes a first transistor, the memory cell further comprising a second branch that includes:

third and fourth switchable resistance legs coupled in parallel with each other and having different resistance values with the predetermined first difference;

a second programming resistor connected to the third and fourth switchable resistance legs and having an unprogrammed, third resistance value and a programmed, fourth resistance value; and

a second transistor cross-coupled with the first transistor.